specification and claim(s) by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"

I. General

Initially, it is noted that applicant has not yet received an initialed copy of the PTO-1449 corresponding to the IDS filed August 10, 2001. Thus, it is respectfully requested that the Examiner confirm consideration of that IDS, and provide the undersigned with an initialed copy of the PTO-1449 corresponding to the same.

It is respectfully requested that the Examiner acknowledge applicant's foreign priority claim under 35 U.S.C. Section 119, and also acknowledge the fact that the USPTO has received a certified copy of the priority document. The certified copy of the priority document was filed with the instant application on August 10, 2001.

II. Example Non-Limiting Embodiments (for ease of understanding)

For purposes of example only, and without limitation, certain example embodiments of this invention relate to a semiconductor memory device. Referring to the embodiment of Figs. 1 and 73 for example, a semiconductor memory device includes a plurality of memory cells (e.g., EEPROMs) stacked on semiconductor substrate 100. As shown in Figs. 1 and 73, an example memory cell includes an island-shaped semiconductor layer(s) 110 which extends vertically relative to the semiconductor substrate 100, a charge storage layer(s) (e.g., floating gate 510), and a control gate(s) 520. It can be seen from Figs. 1 and 73 that the charge storage layer 510 (or 513) and the control gate 520 (or 523) laterally surround a vertically extending sidewall of island-like semiconductor layer 110 as viewed from above. Insulating layer 610 (or 613), including

one or more insulators, is located between the control gate 520 (or 523) and the charge storage layer 510 (or 513). In Fig. 78, a pair of memory cells are located in the central portion of the stack, while first and second selection transistors using gate electrodes 500 are located at the top and bottom of the stack, respectively.

According to certain example non-limiting embodiments of this invention, the active region of at least one of the memory cells in the stack is electrically insulated form the semiconductor substrate 100 (e.g., pg. 47, lines 4-28; pg. 48, lines 4-18; pg. 92, lines 10-14; pg. 95, lines 11-27). In the Fig. 73 embodiment, for example, diffusion layer 710 and/or diffusion layer 720 are provided so that the active regions of the memory cell(s) are in a floating state (electrically insulated) with respect to semiconductor substrate 100 (e.g., pg. 92, lines 10-14). In the Fig. 97-98 embodiment, the island-like semiconductor layer 110 and the semiconductor substrate 100 become in an electrically floating state due to a depletion layer formed on the substrate or semiconductor layer of a PN junction formed between diffusion layer 710 and substrate 100 or semiconductor layer 110 by a difference between a potential given to diffusion layer 710 and a potential given to substrate 100 at times of reading and/or erasing (e.g., pg. 95, lines 11-27). In the Fig. 119, 121 embodiments, impurity diffusion layer(s) 3710 and/or 3721 is/are formed so that active regions of the memory cells are in a floating state with respect to semiconductor substrate 3100 (e.g., pg. 98, lines 3-10). Such structure is advantageous in that a back-bias effect in a semiconductor memory having charge storing layer(s) and control gate(s) can be reduced, and capacity between floating gates and control gates may be increased

without significantly increasing the occupied area and variations in characteristics of memory cells may be suppressed (e.g., pg. 16, lines 19-24).

III. Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Kobayashi (US 6,501,125). This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "a first conductivity type semiconductor substrate; and one or more memory cells comprising an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer, wherein an active region of at least one of said memory cells is electrically insulated from the semiconductor substrate." For example, and without limitation, see Figs. 1 and 73 of the instant application which illustrate that the charge storage layer 510 (or 513) and the control gate 520 (or 523) at least partially laterally surround a sidewall of island-like semiconductor layer 110 as viewed from above. The cited art fails to disclose or suggest the aforesaid underlined aspects of claim 1.

Kobayashi discloses a semiconductor device including a memory cell. In Figs. 1-15 (see especially Fig. 15), Kobayashi illustrates semiconductor substrate 101, isolation regions 102, source/drain diffusion regions 106, floating gate 104c, 111c, insulator 113, control gate 114, and insulators 115, 121. However, Kobayashi differs from the invention of claim 1 in at least the following three respects: (1) Kobayashi's control gate 114 does not partially or fully encircle any sidewall of semiconductor layer 101; i.e., no

sidewall of any semiconductor layer is partially or fully encircled by Kobayashi's floating gate 114; (2) Kobayashi does not disclose or suggest a charge storage layer which partially or fully encircles a sidewall of a semiconductor layer; and (3) Kobayashi's active region is not electrically insulated from semiconductor substrate 101. Instead, semiconductor substrate 101 in Kobayashi is part of the memory cell, thereby teaching directly away from the invention of claim 1. For at least these three reasons, Kobayashi is entirely unrelated to the invention of claim 1 and cannot anticipate or otherwise render it unpatentable.

Claim 1 also stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Yoshida (US 6,483,136). This Section 102(e) rejection is respectfully traversed for at least the following reasons. Yoshida discloses a memory cell which includes both a storage capacitor C and a selection transistor (e.g., col. 8, lines 30-39). In Fig. 4, the selection transistor is at the lower portion of the figure, and the storage capacitor C used for memory is located at the very top of the figure. The storage capacitor C, which is what is apparently used for memory in Yoshida, includes lower capacitor electrode 22, upper capacitor electrode 24, and capacitor insulator 23. The Examiner seems to contend that upper capacitor electrode 24 is a control gate.

However, Yoshida differs from the invention of claim 1 in at least the following two respects: (i) first, the alleged control gate (upper capacitor electrode 124) of Yoshida does not partially or entirely encircle any sidewall of an island-like semiconductor layer; (ii) second, Yoshida's alleged charge storage layer 22 does not partially or fully encircle any sidewall of any island-like semiconductor layer. Thus, it can be seen that Yoshida is

entirely unrelated to the invention of claim 1, and cannot anticipate or otherwise render it unpatentable.

IV. Claim 36

Claim 36 requires "a first conductivity type semiconductor substrate; at least one memory cell comprising an island-like semiconductor layer, a charge storage layer and a control gate, wherein the charge storage layer and the control gate entirely or partially laterally surround at least a portion of a sidewall of the island-like semiconductor layer; and wherein an active region of said memory cell is electrically insulated from the semiconductor substrate." The cited art fails to disclose or suggest these underlined aspects of claim 36.

V. Claim 46

Claim 46 requires "at least one memory cell comprising a pillar-shaped semiconductor layer having a height dimension greater than a width dimension, a charge storage layer and a control gate, wherein the charge storage layer and the control gate entirely or partially laterally surround at least a portion of a sidewall of the pillar-shaped semiconductor layer, wherein the sidewall of the pillar-shaped semiconductor layer extends vertically relative to the semiconductor substrate." The cited art fails to disclose or suggest the aforesaid underlined aspect of claim 46.

VI. Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph beginning at page 95, line 6:

In the example of Fig. 97 and Fig. 98, the source diffusion layer 710 is disposed so that the semiconductor substrate 100 is connected to the island-like semiconductor layer 110, and the diffusion layer 720 is disposed so that the active regions of adjacent transistors are connected to each other in the island-like semiconductor layer 110. The island-like semiconductor layer 110 and the semiconductor substrate [110]100 becomes in an electrically floating state owing to a depletion layer formed on a semiconductor substrate or an island-like semiconductor layer of a PN junction formed between the source diffusion layer 710 and the semiconductor substrate 100 or the island-like semiconductor layer 110 by a difference between a potential given to the source diffusion layer 710 and a potential given to the semiconductor substrate 100 at reading or at erasing. The active regions of the adjacent transistors are electrically insulated from each other owing to a depletion layer formed in the island-like semiconductor of the PN junction formed between the diffusion layer 720 and the island-like semiconductor layer 110 by a difference between the potential given to the diffusion layer 720 and a potential given to the island-like semiconductor layer 110.

IN THE CLAIMS

Cancel non-elected claims 20-28, without prejudice in view of the Restriction Requirement.

1. (Amended) A semiconductor memory comprising:

a first conductivity type semiconductor substrate; and

one or more memory cells [constituted of]comprising an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein an active region of at least one of said [one or more]memory cells is electrically insulated from the semiconductor substrate.

2. (Amended) A semiconductor memory according to claim 1, wherein said active region of said at least one memory cell is electrically insulated from the semiconductor substrate by a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, or by a second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed in the second conductivity type impurity diffusion layer.

4. (Amended) A semiconductor memory according to claim 1, wherein the active region of said memory cell is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer and

a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

5. (Amended) A semiconductor memory according to claim 1, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer, and an active region of at least one of the memory cells is electrically insulated from another memory cell by a second conductivity type impurity diffusion layer formed in the semiconductor substrate or the island-like semiconductor layer and a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

13. (Amended) A semiconductor memory according to claim 1, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer, and an electrode for electrically connecting [cannel]channel layers of memory cells is further formed between control gates.

19. (Amended) A semiconductor memory according to claim 1, wherein a lower gate electrode of a selection transistor, the control gate of the memory cell, and[/or] an

upper gate electrode of another selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate[, and

the upper gate electrode, the control gate and/or the lower gate electrode are sequentially led out to a surface of the semiconductor memory at an end of a memory cell array in which island-like semiconductor layers with the memory cells formed thereon are arranged in matrix].

Please add the following new claims:

29. (New) The semiconductor memory of claim 1, wherein the control gate and the charge store layer each laterally surround a portion of the sidewall of the island-like semiconductor layer on all lateral sides thereof.

30. (New) The semiconductor memory of claim 1, wherein the active region of the one memory cell is electrically insulated from the semiconductor substrate by at least one diffusion layer which is formed at a bottom portion of the island-like semiconductor layer.

31. (New) The semiconductor memory of claim 1, wherein the active region of the one memory cell is electrically insulated from the semiconductor substrate by at least a diffusion layer formed in a top portion of the semiconductor substrate immediately under the island-like semiconductor layer.

32. (New) The semiconductor memory of claim 1, wherein the island-like semiconductor layer is pillar-shaped so as to have a height dimension greater than a width dimension.

33. (New) The semiconductor memory of claim 32, wherein the island-like semiconductor layer has a circular cross section when viewed from above.

34. (New) The semiconductor memory of claim 1, wherein the semiconductor memory is an EEPROM.

35. (New) The semiconductor memory of claim 1, wherein said sidewall of the island-like semiconductor layer is vertically extending relative to a surface of the semiconductor substrate.

36. (New) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

at least one memory cell comprising an island-like semiconductor layer, a charge storage layer and a control gate, wherein the charge storage layer and the control gate entirely or partially laterally surround at least a portion of a sidewall of the island-like semiconductor layer; and

wherein an active region of said memory cell is electrically insulated from the semiconductor substrate.

37. (New) A semiconductor memory according to claim 36, wherein said active region of said memory cell is electrically insulated from the semiconductor substrate by at least a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer.

38. (New) A semiconductor memory according to claim 36, wherein the active region of said memory cell is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, and

a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

39. (New) The semiconductor memory of claim 36, wherein the control gate and the charge store layer each laterally surround at least said portion of the sidewall of the island-like semiconductor layer on all lateral sides thereof.

40. (New) The semiconductor memory of claim 36, wherein the active region of the memory cell is electrically insulated from the semiconductor substrate by at least one

diffusion layer which is formed at a bottom portion of the island-like semiconductor layer.

41. (New) The semiconductor memory of claim 36, wherein the island-like semiconductor layer is pillar-shaped so as to have a height dimension greater than a width dimension.

42. (New) The semiconductor memory of claim 41, wherein the island-like semiconductor layer has a circular cross section when viewed from above.

43. (New) The semiconductor memory of claim 36, wherein the semiconductor memory is an EEPROM.

44. (New) The semiconductor memory of claim 36, wherein said sidewall of the island-like semiconductor layer is vertically extending relative to a surface of the semiconductor substrate.

45. (New) The semiconductor memory of claim 36, wherein a plurality of memory cells are stacked on top of one another over the semiconductor substrate and each use the island-like semiconductor layer, and wherein respective active regions of each of the memory cells are electrically insulated from the semiconductor substrate.

46. (New) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

at least one memory cell comprising a pillar-shaped semiconductor layer having a height dimension greater than a width dimension, a charge storage layer and a control gate, wherein the charge storage layer and the control gate entirely or partially laterally surround at least a portion of a sidewall of the pillar-shaped semiconductor layer, wherein the sidewall of the pillar-shaped semiconductor layer extends vertically relative to the semiconductor substrate; and

wherein at least a portion of the pillar-shaped semiconductor layer of the memory cell is electrically insulated from the semiconductor substrate.

47. (New) A semiconductor memory according to claim 46, wherein said portion of the pillar-shaped semiconductor layer is electrically insulated from the semiconductor substrate by at least a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the pillar-shaped semiconductor layer.

48. (New) A semiconductor memory according to claim 46, wherein said portion of the pillar-shaped semiconductor layer is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the pillar-shaped semiconductor layer, and

a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the pillar-shaped semiconductor layer.

49. (New) The semiconductor memory of claim 46, wherein the control gate and the charge store layer each laterally surround at least said portion of the sidewall of the pillar-shaped semiconductor layer on all lateral sides thereof.

50. (New) The semiconductor memory of claim 46, wherein the pillar-shaped semiconductor layer has a circular cross section when viewed from above.

51. (New) The semiconductor memory of claim 46, wherein the semiconductor memory is an EEPROM.

52. (New) The semiconductor memory of claim 46, wherein a plurality of memory cells are stacked on top of one another over the semiconductor substrate and each use the pillar-shaped semiconductor layer, and wherein respective active regions of each of the memory cells are electrically insulated from the semiconductor substrate.